VC Router Design For Power Efficient Network On Chips

Ashish A Mulajkar and Govind S Patel

School of Electronics and Electrical Engineering,
Lovely Professional University, Phagwara, Punjab, India

Abstract:

The work presented in this paper is analysis and design of power efficient Network on Chips (NoCs). NoC architecture, routers, structure of NoC, topologies and their components has been discussed in this work. The parameters likely speed, latency, static and dynamic power is analyzed. This work found better results as compared to previous works.

Keywords: Network on Chip, Router, topology, latency.

I. INTRODUCTION

Now a day's Network-on-chip has become essential modules in router design with far better results as compared with SoCs (System on chips). NoC is a better option to the bus based and ad hoc based seen in previous designs [2].It provides low scalability, less latency and power among PEs (processing elements) connected on chip. The advanced bypass path technique is used in case of low traffic which reduces latency in the arrival of packets [3].

Area occupancy in the on chip design should also be reduces to improve the performance of the chip. To discard cost of buffers an EB (Elastic Buffer) control technique is used in router design [4].The use of Virtual Channel VCs [7] lowers area, latency as well as static and dynamic power of the chip. The parameters involved in efficient router design involve Buffers, Arbiter, Virtual Channel Controller, Routing path Controller and Allocator [13].

Using power gating method the static power can be reduced. An advanced technique of a VC router called as Easy pass (EZ-Pass) router is discussed that improves power loss by reducing latency among the flits.

II. NETWORK ON CHIP

The typical bus concept implementation requires large Multiplexers and to solve problems of Cache coherence. Hence the bus based communications are not scalable for today's MPSoC structures [6]. The following figure 1 shows the architectural paradigm shift from buses to network.

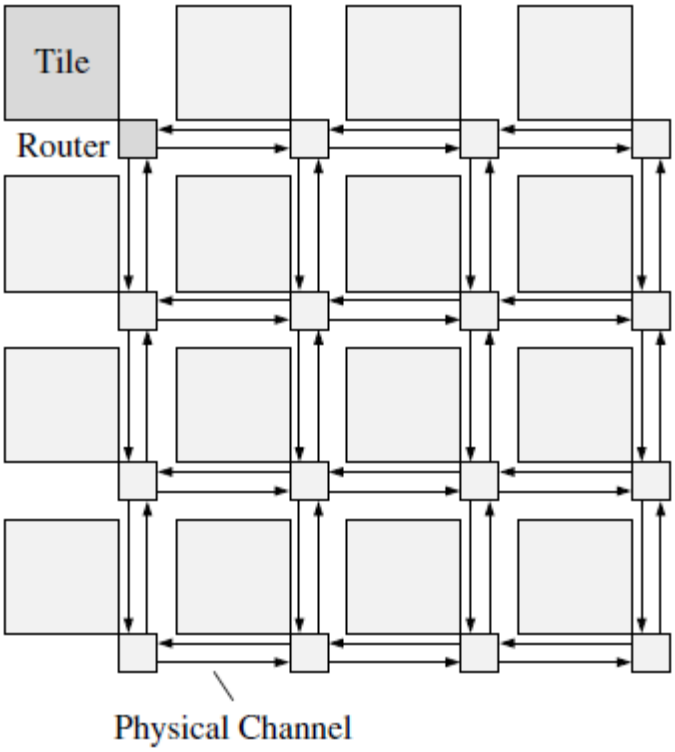

Figure 1. Network on Chip

Similarly, as the numbers of cores in the processor increases, interconnection wire N/W between the cores plays a major role in chip multiprocessors (CMPs) overall performance.

On Chip router design aims to lower count of buffers [5] to increase SoC usable area. Control area overheads can be hided to reduce latency significantly. Impact related to less buffering also shrinks latency in router design by use of single cycle design. Proposed architecture shown in figure 1 is to solve the problems of wider chip area design is to use point to point channels in communication networks. Hence there is reduction in signal loss, power loss and delay in the system. The VC network model is analyzed using Hierarchical Architectural Simulation Environment (HASE).In entire simulation results we consider only single cycle implementation of router. The results are calculated for restricted/unrestricted cross bar implementations.

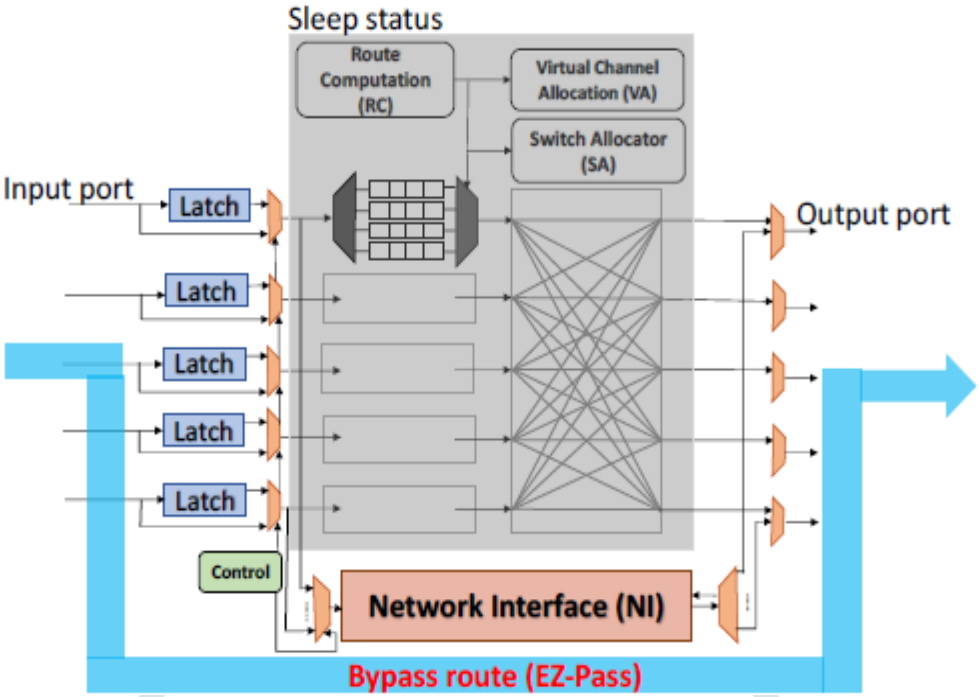

Figure 2. VC Router along with EZ-Pass Router

Figure 2 shows combination of VC Router which is used at when incoming flits maximum while EZ-Pass router is used when traffic is relatively low. The main advantage of this architecture is that the input flits can be routed without disturbing the inactive routers which are powered off during low traffic [14].The EZ Pass route consists of MUX, DEMUX and single flit latches. The Control logic helps the incoming flits to reach NI (Network Interface) rather than moving towards the VC Router. Finally the NI transfers the flits to its respective output port destination. As compared with conventional router, EZ Pass router requires less power and improves the performance of the system. The gem5 simulator is used for simulation purpose. Also to analyze power consumption and router area DSENT has been used.

Finally, the work has been analyzed various topologies with their respective parameters and found good comparative results.

III. CONCLUSION

A low cost technique to improve the performance of the NoC router is achieved by reduction of cycle time. The latency of the router is reduced significantly without hampering the efficiency of router. The EZ Pass routing technique reduces static as well as dynamic power without disturbing the in-active routers. The results shows that static power is reduced by 31% while latency is reduced by 32%

REFERENCES:

[1] Kumar, A., Peh, L. S., Kundu, P., & Jha, N. K. (2007, June). Express virtual channels: towards the ideal interconnection fabric. In ACM SIGARCH Computer Architecture News (Vol. 35, No. 2, pp. 150-161).

[2] Jain, T. N., Ramakrishna, M., Gratz, P. V., Sprintson, A., & Choi, G. (2011). Asynchronous bypass channels for multi-synchronous nocs: A router microarchitecture, topology, and routing algorithm. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 30(11), 1663-1676.

[3] Xin, L., & Choy, C. S. (2010, May). A low-latency NoC router with lookahead bypass. In Proceedings of 2010 IEEE International Symposium on Circuits and Systems (pp. 3981-3984).

[4] Michelogiannakis, G., & Dally, W. J. (2013). Elastic buffer flow control for on-chip networks. IEEE Transactions on computers, 62(2), 295-309.

[5] Mullins, R., West, A., & Moore, S. (2004, June). Low-latency virtual-channel routers for on-chip networks. In Proceedings. 31st Annual International Symposium on Computer Architecture, 2004. (pp. 188-197).

[6] Soteriou, V., Ramanujam, R. S., Lin, B., & Peh, L. S. (2009). A high-throughput distributed shared-buffer NoC router. IEEE Computer Architecture Letters, 8(1), 21-24.

[7] Jose, J., Shankar, J. S., Mahathi, K. V., Kumar, D. K., & Mutyam, M. (2011, December). BOFAR: buffer occupancy factor based adaptive router for mesh NoCs. In Proceedings of the 4th International Workshop on Network on Chip Architectures (pp. 23-28).

[8] Mondal, H. K., Gade, S. H., Kaushik, S., & Deb, S. (2017). Adaptive multi-voltage scaling with utilization prediction for energy-efficient wireless NoC. IEEE Transactions on Sustainable Computing, 2(4), 382-395.

[9] Zheng, H., & Louri, A. (2018). EZ-Pass: An Energy & Performance-Efficient Power-Gating Router Architecture for Scalable NoCs. IEEE Computer Architecture Letters, 17(1), 88-91.

[10] Mondal, H. K., Gade, S. H., Kishore, R., & Deb, S. (2015, December). Power-and performance-aware fine-grained reconfigurable router architecture for NoC. In 2015 Sixth IEEE International Green and Sustainable Computing Conference (IGSC) (pp. 1-6).

[11] Li, C., Dong, D., Lu, Z., & Liao, X. (2018). RoB-Router: A Reorder Buffer Enabled Low Latency Network-on-Chip Router. IEEE Transactions on Parallel and Distributed Systems, 29(9), 2090-2104.

[12] Reehal, G., & Ismail, M. (2014). A systematic design methodology for low-power nocs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 22(12), 2585-2595.

[13] Zheng, H., & Louri, A. (2017). Ez-pass: An energy & performance-efficient power-gating router architecture for scalable nocs. *IEEE Computer Architecture Letters*, *17*(1), 88-91.