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OPTIMUM DECIMATION AND FILTERING FOR RECONFIGURABLE SIGMA DELTA ADC

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Abstract

The Sigma Delta Analog to Digital Converter (SD-ADC) with passive analog components is presented. The digital blocks required for creating the samples with required sample rate and word length from the 1 bit ADC output are presented. The digital filters are initially modeled in MATLAB Simulink and validated in frequency domain. Further they are synthesized to Xilinx Spartan-6 FPGA technology. The synthesis results report clock speeds up to 300MHz. The simulation results are used to validate the principle and verify the

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performance of SD-ADC. The results demonstrate a promising technology area of realizing SD-ADC as a reconfigurable block on FPGA to meet several signal processing applications with sampling rates up to few hundreds of KHz.

1. Sigma Delta ADC

The Sigma Delta Analog to Digital Converter (SD-ADC) is highly preferred ADC architecture in audio, biomedical and several high precision digitization applications. The thrust towards wireless and battery powered applications, motivates the research on low power SD-ADCs. As a result there are several single channel and multi channel ADC chips available in market. Simultaneously the System on Chip (SOC) approach research aims to build the single chip solution incorporating right from data converters to digital processors, employing state of the art VLSI technologies. The necessity of reconfigurability in SoC context is visualized more than a decade before [1] to address wide range of applications. In the programmable or configurable hardware the silicon resources must be useful to build required functionality based on the application. The digital blocks realization using configurable cells is well proven and in usage form decades in FPGAs. The programmability of analog blocks is yet to be established in the industry. Towards the goal of establishing the reconfigurable ADCs, the SD-ADC becomes the preferred option. The feature of digital dominated design of SD-ADC makes it different from other types of ADCs [2].

The limitations of using a separate ADC chip for data conversion are presented at [3]. The architecture simulated at [3] establishes the proof of concept for passive analog component based SD-ADC configured in FPGA. Detailed design analysis of such SD-ADC is carried out in context of both Xilinx [2, 4] and Altera [6] FPGAs. The passive analog only, architectures [2, 4] attempt to implement the Sigma Delta ADCs with minimum passive analog components around low-voltage positive emitter coupled logic (LVPECL) standard FPGA differential pins, while the digital logic is implemented as an Intellectual Property(IP) blocks in FPGA fabric.

The work contributed by Altera group [6] uses FPGA I/O pads with low-voltage differential signaling (LVDS) as a comparator. The differential input pin is faster in comparison with single ended input pin when used as comparator. This is applicable for both Xilinx and Altera FPGAs.

The recently launched IP by Xilinx is another example [5] of such implementation. These IP blocks are envisaged to be FPGA vendor provided allowing the end user to simply instantiate the IP and connect external passive components to realize ADC. The advantage of simplifying the ADC realization brings down the printed circuit board (PCB) design costs and improves reliability.

The work presented in [7, 8] describes the Sigma Delta ADC blocks including the decimation filters. The system generator based simulation results are presented. However the analog signal interfacing blocks are modeled with Simulink models and no practical implementation aspects are discussed. The paper given at [9] also describes only the FPGA prototyping of the Sigma Delta ADC, but aimed for complete ASIC implementation.

In the context of external analog passive type SD-ADC, the digital [3] section accepts the 1 bit ADC output sampled at clock speed of differential pin. In this paper, the work pertaining to digital blocks implementation is presented. The remaining part of paper is organized in three sections. Section 2 elaborates the selected decimator architecture in the context of SD-ADC. Section 3 has the implementation details of the same with the simulation results and conclusions are given in Section 4.

2. CIC Based Decimator

2.1. Decimator in context of SD-ADC

The context of proposed SD-ADC architecture is illustrated in Figure 1. It is derived from previous work [2] with more insight in implementation details.

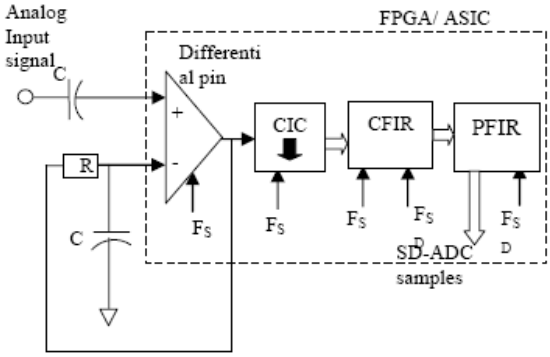

Figure 1. High level block diagram of SD-ADC.

The differential pin is used as comparator which is fed with analog input signal and Integrated Digital Representative of Analog signal (referred as IDRA signal [2]). The input signal is continuously compared with the IDRA signal to produce logic output '1' when input analog signal is higher than IDRA and logic '0' otherwise.

The closed loop established through the negative input of differential pin is controlled through the clock applied to it. As the differential input voltage between positive and negative inputs is less than the rated value [10] (0.25V for LVPECL) we cannot operate at full clock speeds. The rate at which the differential pin output can be read becomes a crucial parameter (assuming the analog counter parts are made to work at those speeds) for deciding the highest possible oversampling for a targeted ADC sampling rate. This rate depends on technology factors with which the ASIC/FPGA is realized.

Based on the HSPICE analysis carried out in [2] it is proposed to work at 200MHz clock speed. As Spartan-6 VLSI technology is much advanced than Virtex-4 device technology this is valid assumption.

Another important aspect of SD-ADC is the allowed dynamic range of input analog signal over which valid digital output words are produced. The dynamic range is limited by the acceptable common mode voltage range for the differential input pin. The unconventional use of differential pin in the proposed manner is not documented by the device manufacturers, hence the worst case input swing of 0.25V for LVPECL is considered here.

The intuitive analysis of output bits produced by differential pin is helpful to validate the results produced by further simulations. If the input signal is rising (positive slope), then there will be more ‘1’s than ‘0’s in the bit stream. Likewise, for signal falling (negative slope), there will be more “0”s than “1”s in the bit stream. For a signal which maintains a constant value, there will be approximately an equal number of “1”s and “0”s. The density of “ones” at the modulator output is proportional to the positive rise in input signal. The basic principle of noise shaping of SD-ADC is described in below section.

The purpose of the integrator in the feedback path is to maintain the average output of the integrator near to the input signal level. For an increasing input the comparator generates a greater number of “ones,” and vice versa for a decreasing input. By summing the error voltage, the integrator acts as a low pass filter to the input signal and a high pass filter to the quantization noise. Thus, most of the quantization noise is pushed into higher frequencies.

It is to be noted that oversampling has changed not the total noise power, but noise distribution over the frequency. The decimation filter applied to the noise-shaped Delta-Sigma modulator, removes more noise than does simple oversampling. Figure 2 illustrates this principle.

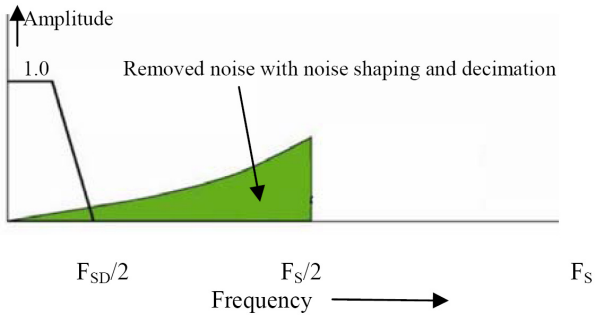

Figure 2. Noise shaping achieved in SD-ADC.

2.2. CIC based decimator

The Cascaded Integrator and Comb (CIC) filters are derived from digital

translation of analog filter sections. The digital version of integrator is accumulator which implements the simplest digital low pass filter. Multiple such sections cascaded results in higher order integration to achieve fast roll off for low pass filter. The *N* stage accumulator has an *N*th order pole at origin. To cancel this pole and to realize stable filter *N* numbers of differentiators are required to be added subsequently. The resultant architecture is referred as CIC. Figure 3 shows the block diagram. The down sampling by factor of *D* is carried out after integrator before comb section.

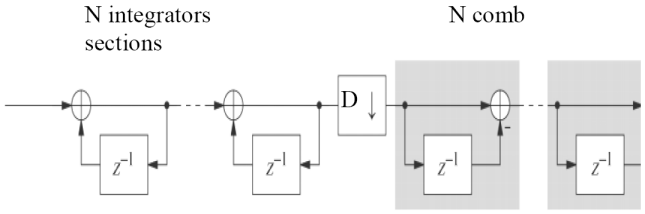

Figure 3. CIC decimator.

3. Simulation Results

The frequency response of CIC filter is decided by the delay in comb sections. This is called *differential delay* in CIC filters. Let this be *M* in the present analysis. The frequency response of the CIC filter can be shown [11] as given in equation (1):

$$|H(f)| = \left| \frac{\sin \pi M f}{\sin \frac{\pi f}{D}} \right|^{N} . \tag{1}$$

The spectrum has nulls at multiples of $f = 1/MD$ in the normalized frequency scale. Also the region around the null is where aliasing is to be considered mainly has very high attenuation. The CIC frequency response with input sampling rate $fs = 1\,\text{MHz}$ (before decimation) for $M = 2$ and $D = 3$ is shown in Figure 4.

It can be seen that the pass band has sinc response after decimation.

The CIC filter does not maintain the flat pass band characteristics; hence a special filter called *Compensation Finite Impulse Response* (*CFIR*) will be used. This maintains an inverse sync frequency response such that the resultant shall have flat pass band. Figure 5 shows the frequency response of the CFIR filter. MATLAB tool is used to compute the inverse sinc function values and used in realizing the filter.

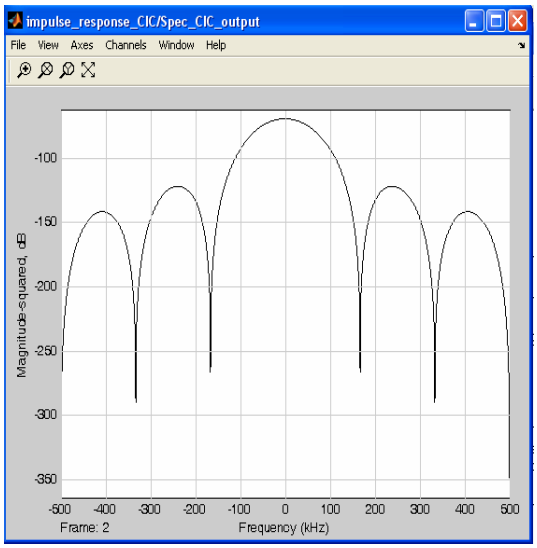

Figure 4. Frequency response of CIC for $M = 2$ and $D = 3$.

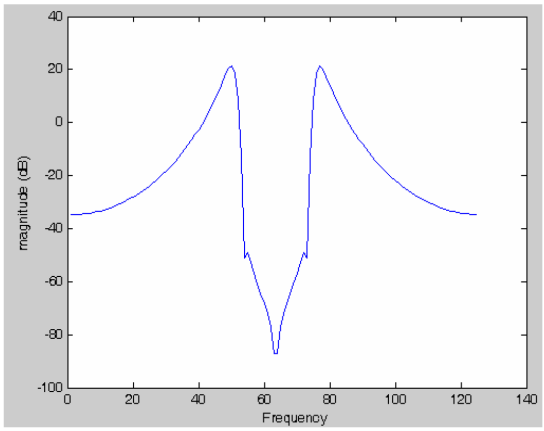

Figure 5. Frequency response of CFIR.

The PFIR filter called *programmable FIR filter* can be used for any further fine frequency selection among the decimated filter bandwidth. Usually 80% to 90% of band only will be used in the decimated bandwidth. This shall be controlled by PFIR filter. To validate the frequency characteristics of decimation filters, they are modeled in fixed point arithmetic in MATLAB Simulink as give in Figure 6.

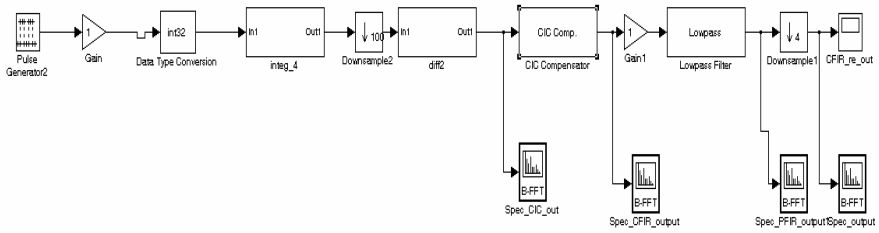

Figure 6. Simulink modeling of CIC based decimator for decimation factor 400.

The CIC filter has gain equal to $(DM)^N$ in its integration stages which results in bit growth. The word length required in the CIC stages can be given through equation (2):

$$WL_{CIC} = N \log_2(DM) + WL_{in}. \tag{2}$$

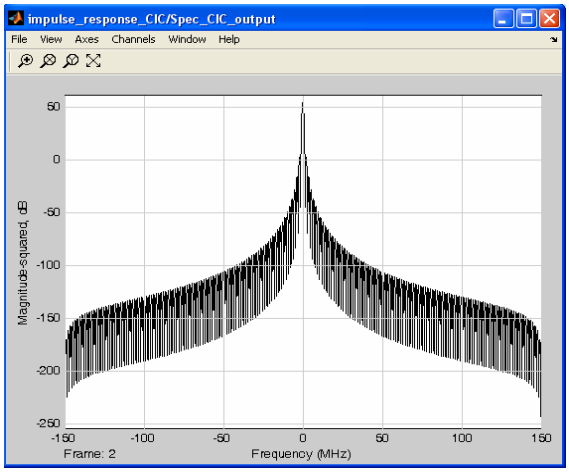

Figure 7. CIC frequency response for $M = 2$, $D = 100$, $N = 4$.

In the case of SD-ADC the input to CIC is from comparator output hence $WL_{in} = 1$. It is proposed to achieve a total decimation of 400. Out of which the decimation of 100 is achieved through CIC filter and remaining 4 is achieved through PFIR filter.

The frequency response of CIC filter for $N = 4$, $M = 2$ and $D = 100$ is shown in Figure 6. Figure 7 shows the zoomed part of Figure 6 at zero frequency. As the resulting sample frequency after decimation by 100 is 3MHz the main lobe of sinc function is spanned between –1.5MHz to +1.5MHz.

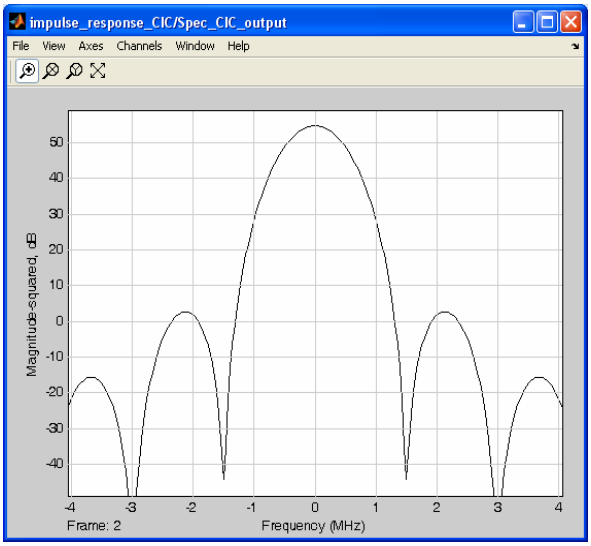

Figure 8. Zoomed at DC for frequency response of Figure 6.

The simulation results obtained through Modelsim tool for sin wave input are shown in Figure 8. The final stage PFIR results show the reconstructed sin wave without any distortions.

The codes are also synthesized using Xilinx Synthesis Technology (XST) tool. The tool reports maximum frequency of operation as 324MHz with 30% area occupied on XC6SLX45T FPGA.

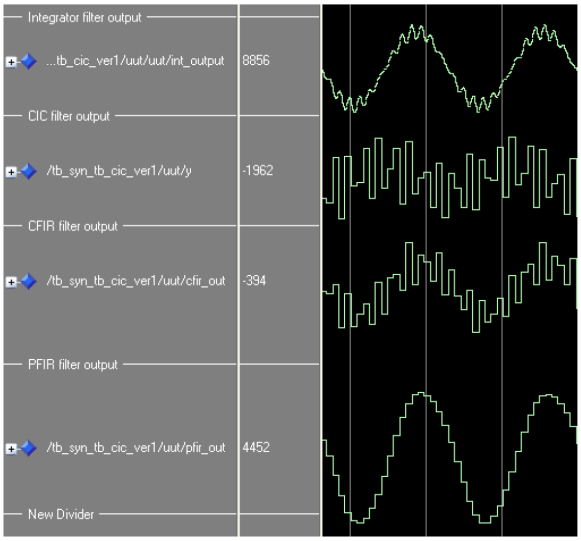

Figure 9. Modelsim simulation results.

4. Conclusion

The digital section of SD-ADC is developed to work at 300MHz input clock speed with decimation of 400. The resulting output clock speed 750KHz is suitable for meeting several instrumentation, audio and SONAR applications. The multiplier less CIC architecture is used to realize front end decimator of 100. An FIR based decimator is configured to generation additional decimation of 4, resulting in total decimation of 400. The work is aimed to be continued in further resource optimization and validation with simulated analog blocks for SD-ADC.

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